REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on September 10, 2003, and the references cited therewith.

No claims are amended or cancelled. Claims 1-48 and 54 remain pending in this application.

§102 Rejection of the Claims

The rejection stated that claims 1, 2, 5, and 6 in so far compliance of 35 U.S.C.112 and as best understood by the Examiner were rejected under 35 USC § 102(e) as being anticipated by Yu (U.S. 6,268,253).

Applicant does not admit that Yu is indeed prior art and reserves the right to swear behind this reference at a later date. Nevertheless the Applicant believes that the present invention is distinguishable from the reference for the following reasons.

The Office Action stated in "Response to Arguments" on Page 8 that, "Applicant argues that Yu does not show oxidizing the gate with sides of the gate dielectric exposed, where portions of the sides of the gate are converted to and oxide. Figures 6 and 7 of Yu's structure clearly shows that the gate oxidized (sic) with sides of the gate dielectric exposed."

Applicant respectfully maintains that Figures 6 and 7 of the Yu reference do not show **oxidizing the gate with sides of the gate dielectric exposed**, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced. Yu appears to show sides of the gate dielectric 202 that are exposed in Figures 6 and 7. Yu also appears to show forming removable spacers 212 in Figure 5 while a gate structure 208 is resting on a **continuous** dielectric layer 202. Applicant stresses that in Figure 5, and as described in column 5, lines 39-50 the dielectric layer 202 is continuous, and no sides of a gate dielectric are exposed. Yu describes removing exposed portions of the layer of gate dielectric 202 **after** formation of the removable spacers 212 (col. 6, lines 1-2).

In contrast, Applicant's present application teaches a method where diffusion through exposed sides of the gate dielectric is controlled. Applicant's independent claim 1 includes oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

Because the Yu reference does not show every element of Applicant's independent claim 1, a 35 USC § 102(e) rejection is not supported. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claim 1. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Claims 7, 8, 14, 15, 18, 19, and 54 were rejected under 35 USC § 102(b) as being anticipated by Xiang et al. (U.S. 5,866,473).

The rejection states that:

> Xiang teaches a method of forming transistor comprising: forming a first source/drain region (212) and a second source/drain region (216) in a semiconductor substrate (204); forming a gate dielectric layer (202) on a semiconductor substrate (204); coupling a barrier layer (206) to the gate dielectric layer wherein the barrier layer prevents oxide undergrowth; forming a gate (208) on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and oxidizing the gate after all source/drain regions have been formed, wherein a portion of the sides of the gate are converted to an oxide (220) and an effective channel length of the gate is reduced (figs. 2A-2F).

Typographical errors found in the previous rejection using the Xiang reference appear to have been carried over once again into the present rejection. For example, element 206 does not appear to be a barrier layer, and element 208 does not appear to be a gate. Applicant has attempted to infer the intent of the rejection, and distinguishes the reference as follows.

Xiang appears to show a gate oxide layer 202 that may include nitrogen (col. 2, lines 46-47). Xiang also appears to show oxidation of a portion of a polysilicon gate electrode 206 to reduce a dimension of the polysilicon gate 206. However, Xiang does not recognize the problem of diffusion from underneath a gate dielectric as discussed in Applicant's specification on page 2, lines 15-30. Further, Xiang does not show, teach or suggest oxidizing the gate **with sides of the gate dielectric exposed**, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

In contrast, Applicant's present application teaches a method where diffusion through exposed sides of the gate dielectric is controlled. Applicant's independent claims 7, 14, and 54

each include oxidizing the gate with sides of the gate dielectric exposed, wherein a portion of the sides of the gate are converted to an oxide and an effective channel length of the gate is reduced.

Because the Xiang reference does not show every element of Applicant's independent claims, a 35 USC § 102(b) rejection is not supported. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 7, 14, and 54. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

§103 Rejection of the Claims

Claims 3, 4, 9, and 16 were rejected under 35 USC § 103(a) as being unpatentable over Yu in view of Gardner (U.S. 6,005,274). Claims 21-23, 25-30, and 32-34 were rejected under 35 USC § 103(a) as being unpatentable over Xiang in view of Gardner. Claims 35-37, 39-44, and 46-48 were rejected under 35 USC § 103(a) as being unpatentable over Xiang in view of Gardner and further in view of Sung et al. (U.S. 6,008,085).

Applicant respectfully submits that the additional references of Gardner and Sung fail to cure the deficiencies of Yu and Xiang as outlined above.

Because the cited references, either alone or in combination, do not show every element of Applicant's independent claims, a 35 USC § 103(a) rejection is not supported by the references. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 3, 4, 9, 16, 21-23, 25-30, 32-37, 39-44, and 46-48. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Claims 10, 17, 24, 31, 38, and 45 were rejected under 35 USC § 103(a) as being unpatentable over Xiang.

Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 because not all of the recited elements of the claims are found Xiang as outlined in the 35 USC § 102 section above. Because all the elements of the claim are not found in the reference, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of official notice with a single reference obviousness rejection

and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests withdrawal of the rejection, or citation of references to cure the deficiencies of Xiang.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6944 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

ZHONGZE WANG ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6944

Date 11-10-03

By _____
David C. Peterson
Reg. No. 47,857

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 10th day of November, 2003.

Amy Moriarty
Name

_____
Signature